Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.039”**

****

**.040”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 x .004” min.**

**Backside Potential: COLLECTOR**

**APPROVED BY: DK DIE SIZE .039” X .040” DATE: 10/4/21**

**MFG: SOLITRON THICKNESS .000” P/N: 2N3439**

**DG 10.1.2**

#### Rev B, 7/1